WHAT IS CLAIMED IS:

1. A method for operating a memory circuit having a plurality of arrays comprising the steps of:

(a) receiving a first command accessing a row in a first array;

(b) opening said first array to allow access to memory cells coupled to said row; and

(c) keeping said first array open until said array receives a second command accessing a different row in said first array.

2. The method of claim 1 further comprising a step of turning off said first array and a second array adjacent to said first array upon receipt of said second command.

3. The method of claim 2 wherein said step of turning off said first array occurs also in response to receipt of a third command accessing a row in said second array adjacent to said first array.

4. A method for operating a memory circuit having a plurality of arrays comprising the steps of:

(a) receiving a command accessing array N;

(b) turning off arrays N, N+1 and N-1;

(c) equilibrating bit lines in array N; and

(d) turning on array N to access a selected word line.

5. A memory circuit comprising:

a plurality of arrays of memory cells, each array having n columns and m rows, with a memory cell coupled at each cross section of a row and a column; and

a plurality of clusters of sense amplifiers, each of said plurality of arrays being sandwiched by a pair of said plurality of clusters of sense amplifiers, each cluster of sense amplifiers having n/2 sense amplifier circuits coupling to n/2 columns in an associated array,

wherein, up to half of said plurality of arrays may be active simultaneously.

6. The memory circuit of claim 5 further comprising a plurality of array enable logic blocks coupled to said plurality of arrays.

7. The memory circuit of claim 6 wherein one of said plurality of array enable logic blocks activates an associated array when a row in said array is selected and keeps said array active until a different row in said array, or a row in an adjacent array is selected.

8. A video chip comprising:

a memory circuit;

controller logic; and

a wide bus coupling said memory circuit to said controller logic,

wherein, said memory circuit comprises:

a plurality of arrays of memory cells, each array having n columns and m rows, with a memory cell coupled at each cross section of a row and a column; and

a plurality of clusters of sense amplifiers, each of said plurality of arrays being sandwiched by a pair of said plurality of clusters of sense amplifiers, each cluster of sense amplifiers having n/2 sense amplifier circuits selectively coupling to n/2 columns in an associated array,

wherein, up to half of said plurality of arrays may be active simultaneously allowing said controller to access more data via said wide bus.

9. The video chip of claim 8 wherein video data representing video display pixel information are stored in said memory circuit whereby data representing one tile is stored in one row per array in non-adjoining arrays.

10. The video chip of claim 8 wherein said plurality of arrays are organized in two or more groups of arrays, and each array comprises at least 1024 columns and at least 256 rows.

11. The video chip of claim 8 wherein said wide bus is at least 128 bits wide.

12. The video chip of claim 9 wherein data comprising any given tile of pixels is stored substantially entirely in either even numbered arrays or substantially entirely in odd numbered arrays.

13. The video chip of claim 9 wherein said data comprising any given tile of pixels is stored in rows that can be simultaneously activated.

14. The video chip of claim 9 wherein data comprising any given screen display line is stored substantially entirely in one row per array in non-adjoining arrays.

15. The video chip of claim 14 wherein said data comprising any given screen display line is stored substantially entirely in either even numbered arrays or substantially entirely in odd numbered arrays.

16. The video chip of claim 15 wherein said data comprising any given screen display line is stored in rows that can be simultaneously activated.

17. The video chip of claim 12 wherein data comprising any given screen display line is stored substantially entirely in either even numbered arrays or substantially entirely in odd numbered arrays.

18. The video chip of claim 17 wherein said data comprising any given tile of pixels is stored in rows that can be simultaneously activated.

19. The video chip of claim 18 wherein said data comprising any given screen display line is stored in rows that can be simultaneously activated.

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